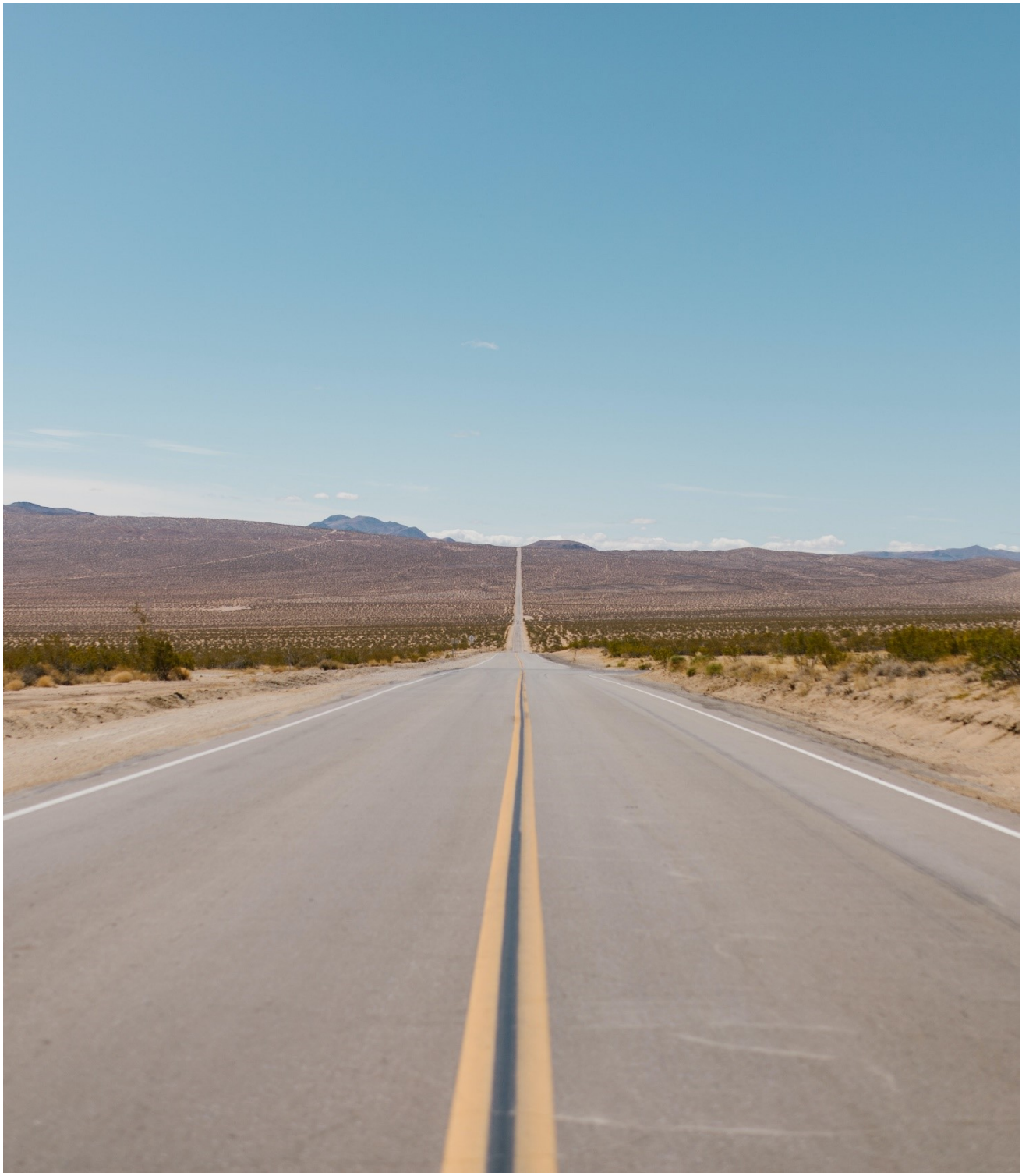
SMH Technologies®

22/01/2025

Driver v. 5.06

Interfacing FlashRunner 2.0 with TEXAS INSTRUMENTS MSPM0

Moreno Ortolan



SMH Technologies S.r.l.

UNIVERSAL PRODUCTION IN-SYSTEM PROGRAMMING

HQ and Registered Office
Via Giovanni Agnelli 1
33083 Villotta di Chions (PN) Italy
Società Unipersonale

Capitale sociale €102.040
P.I. 01697470936
C.F. 01697470936
REA PN-97255

D-U-N-S® 51-724-9350
T + 39 0434 421 111
F + 39 0434 639 021

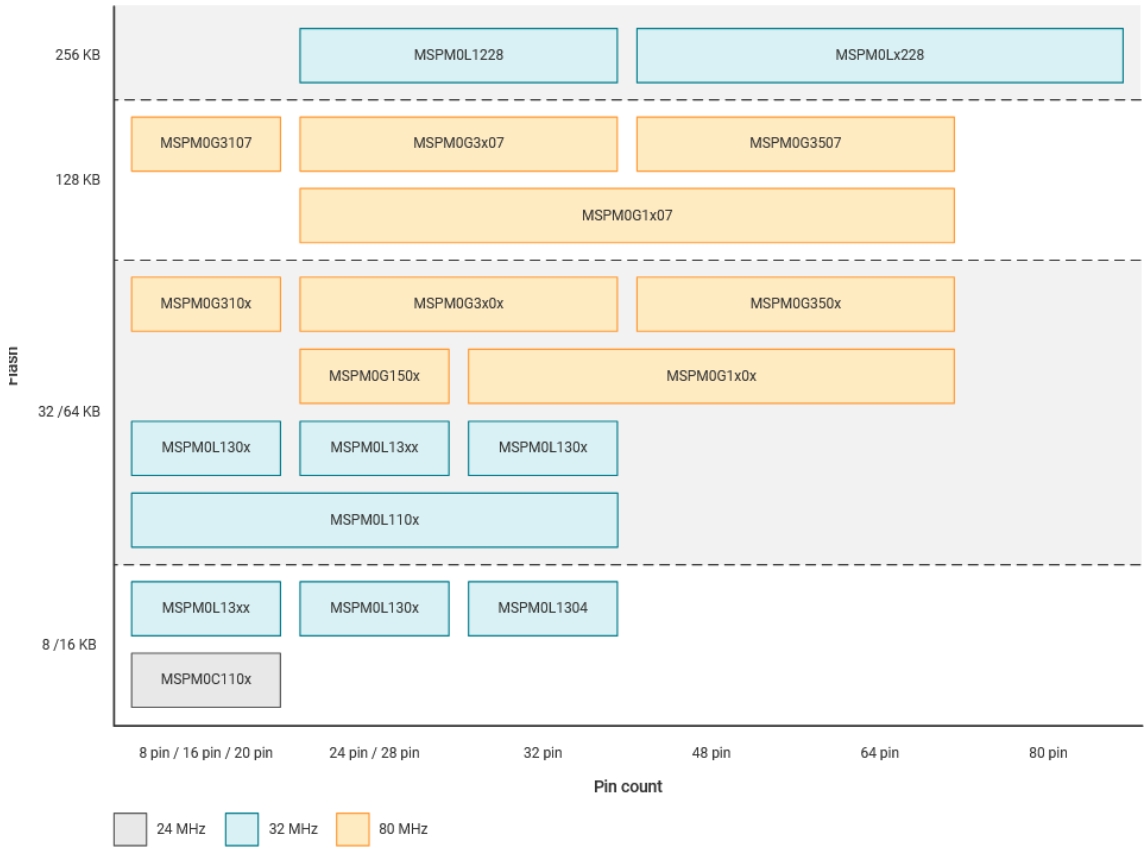
→smh-tech.com

info@smh-tech.com

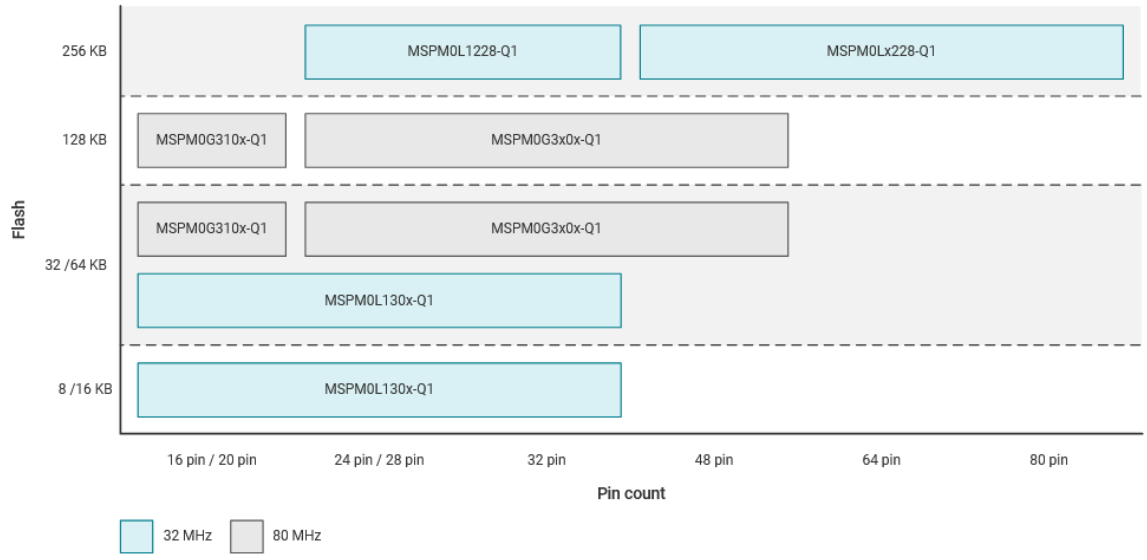
TEXAS INSTRUMENTS MSPM0 Introduction

MSPM0 with Arm Cortex-M0+ MCUs

Industrial MSPM0:



Automotive MSPM0:



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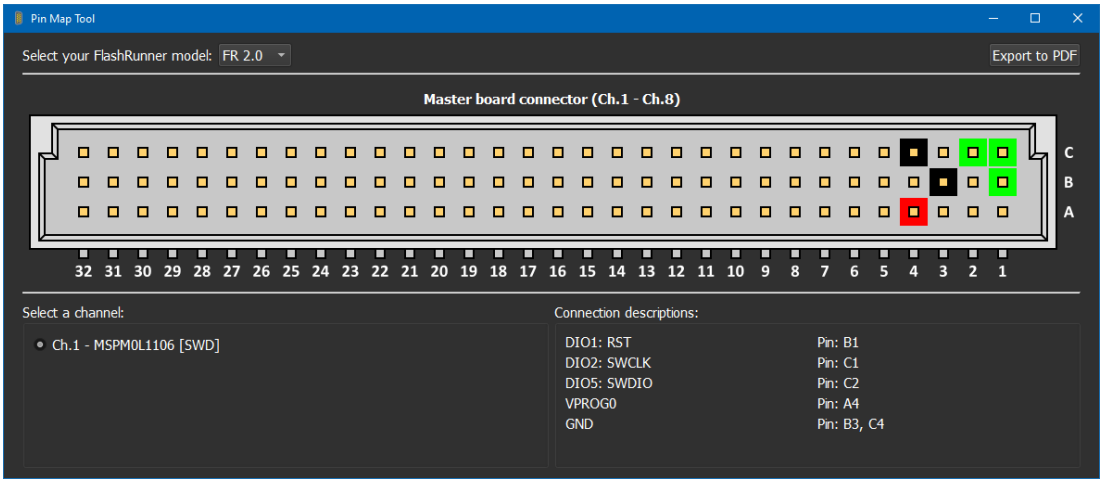
TEXAS INSTRUMENTS MSPM0 Protocol and PIN map

MSPM0 devices support the SWD protocol.

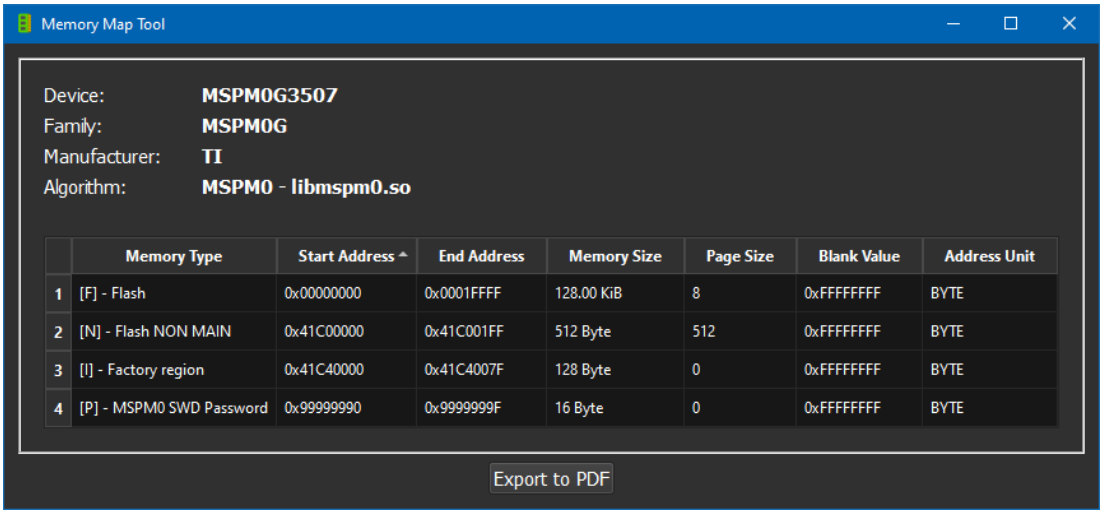
```
#TCSETPAR CMODE <SWD>
```

TEXAS INSTRUMENTS MSPM0 PIN MAP



TEXAS INSTRUMENTS MSPM0 Memory Map

Memory Type	Start Address	End Address	Memory Size	Page Size	Blank Value	Address Unit
[F] – Flash	0x00000000	0x0000FFFF	64.00 KiB	8	0xFFFFFFFF	BYTE
[N] – Flash NON-MAIN	0x41C00000	0x41C001FF	512 Byte	512	0xFFFFFFFF	BYTE
[I] – Factory Region	0x41C40000	0x41C4007F	128 Byte	0	0xFFFFFFFF	BYTE
[P] – MSPM0 SWD Password	0x99999990	0x9999999F	16 Byte	0	0xFFFFFFFF	BYTE



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TEXAS INSTRUMENTS MSPM0 NONMAIN Configuration Memory

The NONMAIN is a dedicated region of flash memory which stores the configuration data used by the BCR and BSL to boot the device.

The region is not used for any other purpose.

The BCR and BSL both have configuration policies which can be left at their default values (as is typical during development and evaluation), or modified for specific purposes (as is typical during production programming) by altering the values programmed into the NONMAIN flash region.

The BCR and BSL configuration data structures are both contained within a single flash sector in the NONMAIN flash memory region. To change any parameter in the boot configuration, it is necessary to erase the entire NONMAIN sector and re-program both the BCR and BSL configuration structures with the desired settings.

The configuration data in the NONMAIN flash region is not affected by a mass erase command, but it is erased and re-programmed to factory defaults by a factory reset command sent to the BCR via the debug sub system mailbox (DSSM) over SWD.

The NONMAIN flash is also erased by a factory reset command sent to the BSL using the UART or I2C BSL interface. However, unlike the DSSM factory reset, the BSL factory reset does not program TI factory defaults to the NONMAIN memory following the erase.

As such, it is the responsibility of the host which is connected to the MSPM0 target (via the BSL interface) to re-program the NONMAIN memory with a valid configuration before terminating the BSL session.

NONMAIN Section	Start Address	End Address
BCR Configuration	0x41C00000	0x41C0005B
BCR Configuration CRC	0x41C0005C	0x41C0005F
BSL Configuration	0x41C00100	0x41C00153
BSL Configuration CRC	0x41C00154	0x41C00157

Please remember to not erase the NONMAIN memory without reprogram it.

From driver version **5.03** a new **#TPCMD** UPDATE_NONMAIN command is available with which it is possible to update the NONMAIN more safely.

Please refer to chapter *TEXAS INSTRUMENTS MSPM0 Driver Commands -> **#TPCMD** UPDATE_NONMAIN* to obtain all the information relating to this command.

In any case you can also execute the following commands:

```
#TPCMD MASSERASE N
#TPCMD BLANKCHECK N
#TPCMD PROGRAM N
#TPCMD VERIFY N R
#TPCMD VERIFY N S
```

If the NONMAIN is left unprogrammed after a factory reset, the device will assume a maximally restrictive state on the next reset cycle, any application code in MAIN flash will not be started, and it will not be possible to access the device via any means.

To prevent lockout, always ensure that valid configuration data is programmed into NONMAIN memory.

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TEXAS INSTRUMENTS MSPM0 NONMAIN Default Values

In this chapter you can see the default values for NONMAIN memory for each series of MSPM0.
The **#TPCMD** UPDATE_NONMAIN command automatically stores these default values in case customer data programming fails.

MSPM0C110x NONMAIN Default Values

Address 41C00000

```
0x03, 0x00, 0x00, 0x00, 0xBB, 0xAA, 0xBB, 0xAA, 0xBB, 0xAA, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF,
0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF,
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```

MSPM0L11xx_13xx NONMAIN Default Values

Address 41C00000

```
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0xBB, 0xAA, 0xBB, 0xAA, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF,
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0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF,
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```

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MSPM0G1x0x_G3x0x NONMAIN Default Values

Address 41C00000

```
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```


HQ and Registered Office
Via Giovanni Agnelli 1
33083 Villotta di Chions (PN) Italy
Società Unipersonale

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D-U-N-S® 51-724-9350
T + 39 0434 421 111
F + 39 0434 639 021

→smh-tech.com
info@smh-tech.com

TEXAS INSTRUMENTS MSPM0 Special SWD Operations

If the MSPM0 device you are programming is locked (AP[0] MCPUSS debug AP is not available) you can perform special operations via SWD Mailbox.

These operations are:

- SWD Masserase (**#TCSETPAR** CONNECT_UNLOCK MAILBOX_MASSERASE)
- SWD Factory Reset (**#TCSETPAR** CONNECT_UNLOCK MAILBOX_FACTORY_RESET)
- SWD Authentication with Password (**#TCSETPAR** CONNECT_UNLOCK MAILBOX_PW_AUTHENTICATION)

If the device is locked and the **#TCSETPAR** CONNECT_UNLOCK parameter is not set, from the log you will see the following behaviour:

```
---#TPCMD CONNECT
Protocol selected SWD.
Trying Hot Plug connect procedure.
IDCODE: 0x6BA02477.
Designer: 0x23B, Part Number: 0xBA02, Version: 0x6.
ID-Code read correctly at 4.00 MHz.
JTAG-SWD Debug Port enabled.
Scanning AP map to find all APs.
AP[0] MCPUSS debug AP is not available. Probably device is locked.
 * TCSETPAR CONNECT_UNLOCK is not set.
 * To enter to the device normally, please set the correct unlock procedure.
 * Connect procedure completed now. No other operations can be performed.
Time for Connect: 0.205 s.
>|
---#TPCMD MASSERASE F
Device is locked. Current command cannot be executed.
Error!|
```

If instead you set the **#TCSETPAR** CONNECT_UNLOCK command with one of the possible inputs you obtain the following results:

CONNECT_UNLOCK MAILBOX_MASSERASE

```
---#TPCMD CONNECT
Protocol selected SWD.
Trying Hot Plug connect procedure.
IDCODE: 0x6BA02477.
Designer: 0x23B, Part Number: 0xBA02, Version: 0x6.
ID-Code read correctly at 4.00 MHz.
JTAG-SWD Debug Port enabled.
Scanning AP map to find all APs.
AP[0] MCPUSS debug AP is not available. Probably device is locked.
 * Initiating Device Masserase.
 * Attempting Security AP connection.
 * Send command to Security AP registers.
 * Start hardware reset using NRST.
   * Set the reset line low.
   * Set the reset line high.
   * Board reset completed.
 * Reconnect to the device.
 * Attempting Security AP connection.
 * Wait until MCPUSS debug AP return operative...
> Command executed correctly.
Scanning AP map to find all APs.
AP[0] IDR: 0x84770001, Type: AMBA AHB3 bus, Description: MCPUSS debug AP.
AP[1] IDR: 0x002E0001, Type: AMBA AHB3 bus, Description: Configuration AP.
AP[2] IDR: 0x002E0000, Type: JTAG connection, Description: Security AP.
AP[3] IDR: 0x002E0003, Type: MEM-AP bus, Description: EnergyTrace™ AP.
AP[4] IDR: 0x002E0002, Type: AMBA APB2 or APB3 bus, Description: Power AP.
AP[0] ROM table base address 0xF0000000.
CPUID: 0x410CC601.
Implementer Code: 0x41 - [ARM].
Found Cortex M0+ revision r0p1.
Program counter value is 0x01000004.
Cortex M0+ Core halted [0.001 s].
Device configuration:
 * Flash main size: 128 KiB.
 * Flash main bank number: 1.
 * SRAM size: 32 KiB.
 * Data Flash size: 0 KiB.
 * Manufacturer ID: 0x017 - Texas Instruments.
```


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```
 * Part Number ID: 0xBB88.
 * Version ID: 0x2.
PLL enabled using internal oscillator.
Requested Clock is 37.50 MHz.
Generated Clock is 37.50 MHz.
Good samples: 4 [Range 4-7].
IDCODE: 0x6BA02477.
Designer: 0x23B, Part Number: 0xBA02, Version: 0x6.
ID-Code read correctly at 37.50 MHz.
Time for Connect: 0.419 s.
>|
```

CONNECT_UNLOCK MAILBOX_FACTORY_RESET

```
---#TPCMD CONNECT
Protocol selected SWD.
Trying Hot Plug connect procedure.
IDCODE: 0x6BA02477.
Designer: 0x23B, Part Number: 0xBA02, Version: 0x6.
ID-Code read correctly at 4.00 MHz.
JTAG-SWD Debug Port enabled.
Scanning AP map to find all APs.
AP[0] MCPUSS debug AP is not available. Probably device is locked.
 * Initiating Device Factory Reset.
 * Attempting Security AP connection.
 * Send command to Security AP registers.
 * Start hardware reset using NRST.
   * Set the reset line low.
   * Set the reset line high.
   * Board reset completed.
 * Reconnect to the device.
 * Attempting Security AP connection.
 * Wait until MCPUSS debug AP return operative...
> Command executed correctly.
Scanning AP map to find all APs.
AP[0] IDR: 0x84770001, Type: AMBA AHB3 bus, Description: MCPUSS debug AP.
AP[1] IDR: 0x002E0001, Type: AMBA AHB3 bus, Description: Configuration AP.
AP[2] IDR: 0x002E0000, Type: JTAG connection, Description: Security AP.
AP[3] IDR: 0x002E0003, Type: MEM-AP bus, Description: EnergyTrace™ AP.
AP[4] IDR: 0x002E0002, Type: AMBA APB2 or APB3 bus, Description: Power AP.
AP[0] ROM table base address 0xF0000000.
CPUID: 0x410CC601.
Implementer Code: 0x41 - [ARM].
Found Cortex M0+ revision r0p1.
Program counter value is 0x01000004.
Cortex M0+ Core halted [0.001 s].
Device configuration:
 * Flash main size: 128 KiB.
 * Flash main bank number: 1.
 * SRAM size: 32 KiB.
 * Data Flash size: 0 KiB.
 * Manufacturer ID: 0x017 - Texas Instruments.
 * Part Number ID: 0xBB88.
 * Version ID: 0x2.
PLL enabled using internal oscillator.
Requested Clock is 37.50 MHz.
Generated Clock is 37.50 MHz.
Good samples: 4 [Range 4-7].
IDCODE: 0x6BA02477.
Designer: 0x23B, Part Number: 0xBA02, Version: 0x6.
ID-Code read correctly at 37.50 MHz.
Time for Connect: 0.419 s.
>|
```


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CONNECT_UNLOCK MAILBOX_PW_AUTHENTICATION

To use this command, you must also add the 128bit password in the **MSPM0 SWD Password** section of the memory map at virtual address 0x99999990.

	Memory Type	Start Address	End Address	Memory Size	Page Size	Blank Value	Address Unit
1	[F] - Flash	0x00000000	0x0001FFFF	128.00 KiB	8	0xFFFFFFFF	BYTE
2	[N] - Flash NON MAIN	0x41C00000	0x41C001FF	512 Byte	512	0xFFFFFFFF	BYTE
3	[I] - Factory region	0x41C40000	0x41C4007F	128 Byte	0	0xFFFFFFFF	BYTE
4	[P] - MSPM0 SWD Password	0x99999990	0x9999999F	16 Byte	0	0xFFFFFFFF	BYTE

To do this, for example, you can use dynamic memory as in the example below:

```
#DYNMEMSET2 0x99999990 16 DEADBEEFC0FFEE00112233445566778 8
```

If no value is defined in the Password memory section, then the default password `FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF` will be used.

```
---#TPCMD CONNECT
Protocol selected SWD.
Trying Hot Plug connect procedure.
IDCODE: 0x6BA02477.
Designer: 0x23B, Part Number: 0xBA02, Version: 0x6.
ID-Code read correctly at 4.00 MHz.
JTAG-SWD Debug Port enabled.
Scanning AP map to find all APs.
AP[0] MCPUSS debug AP is not available. Probably device is locked.
 * Initiating Device Masserase.
 * Attempting Security AP connection.
 * Send command to Security AP registers.
 * Start hardware reset using NRST.
   * Set the reset line low.
   * Set the reset line high.
   * Board reset completed.
 * Reconnect to the device.
 * Attempting Security AP connection.
 * Send password and try to unlock the device.
 * Wait until MCPUSS debug AP return operative...
> Command executed correctly.
Scanning AP map to find all APs.
AP[0] IDR: 0x84770001, Type: AMBA AHB3 bus, Description: MCPUSS debug AP.
AP[1] IDR: 0x002E0001, Type: AMBA AHB3 bus, Description: Configuration AP.
AP[2] IDR: 0x002E0000, Type: JTAG connection, Description: Security AP.
AP[3] IDR: 0x002E0003, Type: MEM-AP bus, Description: EnergyTrace™ AP.
AP[4] IDR: 0x002E0002, Type: AMBA APB2 or APB3 bus, Description: Power AP.
AP[0] ROM table base address 0xF0000000.
CPUID: 0x410CC601.
Implementer Code: 0x41 - [ARM].
Found Cortex M0+ revision r0p1.
Program counter value is 0x01000004.
Cortex M0+ Core halted [0.001 s].
Device configuration:
 * Flash main size: 128 KiB.
 * Flash main bank number: 1.
 * SRAM size: 32 KiB.
 * Data Flash size: 0 KiB.
 * Manufacturer ID: 0x017 - Texas Instruments.
 * Part Number ID: 0xBB88.
 * Version ID: 0x2.
PLL enabled using internal oscillator.
Requested Clock is 37.50 MHz.
Generated Clock is 37.50 MHz.
Good samples: 4 [Range 4-7].
IDCODE: 0x6BA02477.
Designer: 0x23B, Part Number: 0xBA02, Version: 0x6.
ID-Code read correctly at 37.50 MHz.
Time for Connect: 0.419 s.
>|
```


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TEXAS INSTRUMENTS MSPM0 Driver Parameters

The standard parameters are used to configure some specific options inside MSPM0 driver.

#TCSETPAR ENTRY_CLOCK

Syntax: `#TCSETPAR ENTRY_CLOCK <Frequency>`

<Frequency> Accepted parameters 4000000, 2000000, 1000000, 500000, 100000 Hz

Description: Set the SWD frequency used in the Connect procedure before raising the PLL of the device, if the device PLL is available

Note: Default value 4.00 MHz

#TCSETPAR PLL_ENABLED

Syntax: `#TCSETPAR PLL_ENABLED <Value>`

<Value> Accepted parameters YES / NO

Description: Enable the PLL of the device at the highest possible frequency if it's available

Note: Default value YES

#TCSETPAR CONNECT_UNLOCK

Syntax: `#TCSETPAR CONNECT_UNLOCK <Option>`

<Option> Accepted parameters are:

- MAILBOX_MASSERASE
- MAILBOX_FACTORY_RESET
- MAILBOX_PW_AUTHENTICATION

Description: Perform selected unlock procedure during Connect if the device is locked.

Note: Added from driver version **5.01**
Default value NONE

#TCSETPAR SAMPLING_POINT

Syntax: `#TCSETPAR SAMPLING_POINT <Value>`

<Value> Accepted values are in the range 1-15

Description: Use this parameter to permanently set the sampling point of the FPGA
It is recommended to leave this parameter with the default value

Note: Default value 17

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#TCSETPAR I2C_FREQUENCY

Syntax: `#TCSETPAR I2C_FREQUENCY<Value>`

<Value> Accepted values are 10000, 400000 and 1000000

Description: Use this parameter to set the I2C frequency used to communicate with the external memory connected to MSPM0 device

Note: Default value is 400000

#TCSETPAR I2C_SDA_PIN

Syntax: `#TCSETPAR I2C_SDA_PIN <Pin Value>`

<Pin Value> Accepted values are for example **PA**0, **PA**1, **PA**11, ...

Description: Use this parameter to set the SDA pin of I2C peripheral to communicate with the external memory

#TCSETPAR I2C_SCL_PIN

Syntax: `#TCSETPAR I2C_SCL_PIN <Pin Value>`

<Pin Value> Accepted values are for example **PA**0, **PA**1, **PA**11, ...

Description: Use this parameter to set the SCL pin of I2C peripheral to communicate with the external memory

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TEXAS INSTRUMENTS MSPM0 Driver Commands

Here you can find the complete list of all available commands for MSPM0 driver.

```
Memory type:

F → Flash
N → Flash NON-MAIN
I → Factory Region
E → External EEPROM
P → MSPM0 SWD Password (Virtual Address)
```

#TPCMD CONNECT

#TPCMD CONNECT

This function performs the entry and is the first command to be executed when starting the communication with the device.

```
---#TPCMD CONNECT
Protocol selected SWD.
Entry Clock is 4.00 MHz.
Trying Reset Impulse connect procedure.
IDCODE: 0x6BA02477.
Designer: 0x23B, Part Number: 0xBA02, Version: 0x6.
ID-Code read correctly at 4.00 MHz.
JTAG-SWD Debug Port enabled.
Scanning AP map to find all APs.
AP[0] IDR: 0x84770001, Type: AMBA AHB3 bus, Description: MCPUSS debug AP.
AP[1] IDR: 0x002E0001, Type: AMBA AHB3 bus, Description: Configuration AP.
AP[2] IDR: 0x002E0000, Type: JTAG connection, Description: Security AP.
AP[3] IDR: 0x002E0003, Type: MEM-AP bus, Description: EnergyTrace™ AP.
AP[4] IDR: 0x002E0002, Type: AMBA APB2 or APB3 bus, Description: Power AP.
AP[0] ROM table base address 0xF0000000.
CPUID: 0x410CC601.
Implementer Code: 0x41 - [ARM].
Found Cortex M0+ revision r0p1.
Program counter value is 0x0000264C.
Valid Program Counter found into Flash Memory. Forcing software breakpoint.
Breakpoint software used correctly. Program Counter value is 0x0000264C.
Cortex M0+ Core halted [0.013 s].
Device configuration:
 * Flash main size: 64 KiB.
 * Flash main bank number: 1.
 * SRAM size: 4 KiB.
 * Data Flash size: 0 KiB.
 * Manufacturer ID: 0x017 - Texas Instruments.
 * Part Number ID: 0xBB82.
 * Version ID: 0x1.
PLL enabled using internal oscillator.
Requested Clock is 37.50 MHz.
Generated Clock is 37.50 MHz.
Good samples: 3 [Range 5-7].
IDCODE: 0x6BA02477.
Designer: 0x23B, Part Number: 0xBA02, Version: 0x6.
ID-Code read correctly at 37.50 MHz.
Time for Connect: 0.127 s.
>|
```


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#TPCMD MASSERASE

```
#TPCMD MASSERASE <F|N>
```
Use this command to erase the Flash or the NON-MAIN memory.

#TPCMD ERASE

```
#TPCMD ERASE <F|N>
#TPCMD ERASE <F|N> <start address> <size>
```
With this command, a Page Erase of the Flash or the NON-MAIN memory will be performed.
Typically running the Page Erase command takes much longer than running the Masserase command.
Enter the Start Address and Size in hexadecimal format.

#TPCMD BLANKCHECK

```
#TPCMD BLANKCHECK <F|N>
#TPCMD BLANKCHECK <F|N> <start address> <size>
```
Verify if selected part of the Flash or the NON-MAIN memory is erased.
Enter the Start Address and Size in hexadecimal format.

#TPCMD PROGRAM

```
#TPCMD PROGRAM <F|N|E>
#TPCMD PROGRAM <F|N|E> <start address> <size>
```
Program selected part of Flash, NON-MAIN or external EEPROM memory.
Enter the Start Address and Size in hexadecimal format.

#TPCMD VERIFY

```
#TPCMD VERIFY <F|N|E> <R>
#TPCMD VERIFY <F|N|E> <R> <start address> <size>
```
R: Readout Mode.
Verify selected part of Flash, NON-MAIN or external EEPROM memory.
Enter the Start Address and Size in hexadecimal format.

```
#TPCMD VERIFY <F|N> <S>
#TPCMD VERIFY <F|N> <S> <start address> <size>
```
S: Checksum 32 Bit Mode.
Verify selected part of Flash or NON-MAIN memory through Checksum 32Bit method.
Enter the Start Address and Size in hexadecimal format.

#TPCMD READ

```
#TPCMD READ <F|N|E|I>
#TPCMD READ <F|N|E|I> <start address> <size>
```
Read selected part of Flash, NON-MAIN, Factory or external EEPROM memory.
The result of the read command will be visible into the Terminal.
Enter the Start Address and Size in hexadecimal format.

#TPCMD DUMP

```
#TPCMD DUMP <F|N|E|I>
#TPCMD DUMP <F|N|E|I> <start address> <size>
```
Dump selected part of Flash, NON-MAIN, Factory or external EEPROM memory.
The result of the dump command will be stored in the FlashRunner 2.0 internal memory.
Enter the Start Address and Size in hexadecimal format.

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#TPCMD UPDATE_NONMAIN

Syntax: `#TPCMD UPDATE_NONMAIN`

Prerequisites: none

Description: Update the NONMAIN memory using the data from the FRB file or Dynamic memory or both inserted by the customer.
This command is safer than executing `MASSERASE`, `BLANKCHECK`, `PROGRAM` and `VERIFY` in sequence as single commands because everything is executed internally within the kernel inside the MSPM0 device and therefore prevents the NONMAIN memory from remaining unprogrammed or badly programmed if the connection with the device is lost.
If the programming of the NONMAIN memory is not successful with the customer data then the command will automatically try to program the default values to ensure that the memory does not remain in a bad state.

Note: Added from driver version **5.03**

Examples: Correct command execution: 😊

Update NONMAIN memory with customer data successfully:

```
---#TPCMD UPDATE_NONMAIN
Processing input data:
 * Read current NONMAIN memory content.
 * Read FRB file for NONMAIN memory.
 * Write FRB NONMAIN data into RAM memory.
 * Verify FRB NONMAIN data.
 * Write default NONMAIN data into RAM memory.
 * Verify default NONMAIN data.
> Data loaded correctly.
Load kernel to Update NONMAIN memory.
 * Verify kernel loaded.
 * Start kernel loaded.
> Kernel started correctly.
Started NONMAIN update process:
 * NONMAIN erase executed.
 * NONMAIN blankcheck executed.
 * NONMAIN program executed.
 * NONMAIN verify executed.
> Updated NONMAIN process completed.
Time for Update NONMAIN: 0.008 s.
```

Updating NONMAIN memory with customer data failed, running into recovery mode:

```
---#TPCMD UPDATE_NONMAIN
Processing input data:
 * Read current NONMAIN memory content.
 * Read FRB file for NONMAIN memory.
 * Write FRB NONMAIN data into RAM memory.
 * Verify FRB NONMAIN data.
 * Write default NONMAIN data into RAM memory.
 * Verify default NONMAIN data.
> Data loaded correctly.
Load kernel to Update NONMAIN memory.
 * Verify kernel loaded.
 * Start kernel loaded.
> Kernel started correctly.
Started NONMAIN update process:
 * NONMAIN erase executed.
 * NONMAIN blankcheck executed.
 * NONMAIN program executed.
 * NONMAIN update process failed. Try to recover NONMAIN memory.
   * NONMAIN recover mode erase executed.
   * NONMAIN recover mode verify executed.
   * NONMAIN recover mode program executed.
   * NONMAIN recover mode verify executed.
> Updated NONMAIN process completed with recovery mode.
Time for Update NONMAIN: 0.014 s.
```


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#TPCMD GET_DEVICE_INFORMATIONS

Syntax: `#TPCMD GET_DEVICE_INFORMATIONS`

Prerequisites: none

Description: Read Device Informations and print it into Real Time Log and Terminal

Note: Added from driver version **5.00**

Examples: Correct command execution: 😊

```
---#TPCMD GET_DEVICE_INFORMATIONS
Trace ID: 0x00000001.
Manufacturer ID: 0x017.
Part Number ID: 0xBB82.
Version ID: 0x1.
Unique ID part: 0x0000.
Unique ID variant: 0x00.
Unique ID major revision: 0x0.
Unique ID minor revision: 0x0.
UART RXD PIN used by BSL: 0x17.
BSL UART RXD Pin Function selection value: 0x02.
UART TXT PIN used by BSL: 0x18.
BSL UART TXD Pin Function selection value: 0x02.
I2C SDA PIN used by BSL: 0x01.
BSL I2C SDA Pin Function selection value: 0x03.
I2C SCL PIN used by BSL: 0x02.
BSL I2C SCL Pin Function selection value: 0x03.
BSL Invocation Pin Number: 0x13.
GPIO Level used for BSL Pin Invocation: 0x1.
GPIO Pin Selection in GPIO Module: 0x12.
GPIO Module Selection: 0x0.
Main Flash size: 0x040 - 64 KiB.
Main Flash banks number: 0x1.
Sram size: 0x04 - 4 KiB.
Data Flash size: 0x0 - 0 KiB.
Temperature sensor room temperature: 0x00000000.
BOOTCRC: 0xFB1E0F5E.
Time for Get Device Information: 0.005 s
```

#TPCMD GET_TRACE_ID

Syntax: `#TPCMD GET_TRACE_ID`

Prerequisites: none

Description: Read the Trace ID and print it into Real Time Log and Terminal

Note: Added from driver version **5.00**

Examples: Correct command execution: 😊

```
---#TPCMD GET_TRACE_ID
Trace ID: 0x00000001.
Time for Get Trace ID: 0.001 s
```

#TPCMD GET_DEVICE_ID

Syntax: `#TPCMD GET_DEVICE_ID`

Prerequisites: none

Description: Read the Device ID and print it into Real Time Log and Terminal

Note: Added from driver version **5.00**

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Examples: Correct command execution: 😊

```
---#TPCMD GET_DEVICE_ID
Manufacturer ID: 0x017.
Part Number ID: 0xBB82.
Version ID: 0x1.
Time for Get Device ID: 0.001 s
```

#TPCMD GET_USER_ID

Syntax: `#TPCMD GET_USER_ID`

Prerequisites: none

Description: Read the User ID and print it into Real Time Log and Terminal

Note: Added from driver version **5.00**

Examples: Correct command execution: 😊

```
---#TPCMD GET_USER_ID
Unique ID part: 0x0000.
Unique ID variant: 0x00.
Unique ID major revision: 0x0.
Unique ID minor revision: 0x0.
Time for Get User ID: 0.002 s
```

#TPCMD GET_PIN_CONFIG

Syntax: `#TPCMD GET_PIN_CONFIG`

Prerequisites: none

Description: Read the PIN configuration and print it into Real Time Log and Terminal

Note: Added from driver version **5.00**

Examples: Correct command execution: 😊

```
---#TPCMD GET_PIN_CONFIG
UART RXD PIN used by BSL: 0x17.
BSL UART RXD Pin Function selection value: 0x02.
UART TXT PIN used by BSL: 0x18.
BSL UART TXD Pin Function selection value: 0x02.
I2C SDA PIN used by BSL: 0x01.
BSL I2C SDA Pin Function selection value: 0x03.
I2C SCL PIN used by BSL: 0x02.
BSL I2C SCL Pin Function selection value: 0x03.
BSL Invocation Pin Number: 0x13.
GPIO Level used for BSL Pin Invocation: 0x1.
GPIO Pin Selection in GPIO Module: 0x12.
GPIO Module Selection: 0x0.
Time for Get PIn Configuration: 0.003 s
```

#TPCMD GET_FLASH_RAM_SIZE

Syntax: `#TPCMD GET_FLASH_RAM_SIZE`

Prerequisites: none

Description: Read the Flash and RAM size and print it into Real Time Log and Terminal

Note: Added from driver version **5.00**

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Examples: Correct command execution: 😊

```
---#TPCMD GET_FLASH_RAM_SIZE
Main Flash size: 0x040 - 64 KiB.
Main Flash banks number: 0x1.
Sram size: 0x04 - 4 KiB.
Data Flash size: 0x0 - 0 KiB.
Time for Get Flash Ram Size: 0.002 s
```

#TPCMD GET_TEMPERATURE_SENSE

Syntax: `#TPCMD GET_TEMPERATURE_SENSE`

Prerequisites: none

Description: Read the Temperature sense and print it into Real Time Log and Terminal

Note: Added from driver version **5.00**

Examples: Correct command execution: 😊

```
---#TPCMD GET_TEMPERATURE_SENSE
Temperature sensor room temperature: 0x00000000.
Time for Get Temperature Sense: 0.001 s
```

#TPCMD GET_BOOT_CRC

Syntax: `#TPCMD GET_BOOT_CRC`

Prerequisites: none

Description: Read the Boot CRC and print it into Real Time Log and Terminal

Note: Added from driver version **5.00**

Examples: Correct command execution: 😊

```
---#TPCMD GET_BOOT_CRC
BOOTCRC: 0xFB1E0F5E.
Time for Get Boot CRC: 0.001 s
```

#TPCMD RUN

Syntax: `#TPCMD RUN <Time [s]>`

<Time [s]>	Time in seconds (i.e., 2 s). This time is an optional parameter.

Prerequisites: none

Description: Move the Reset line up and down quickly if no parameter <Time [s]> is inserted.
`#TPCMD RUN <Time [s]>` instead moves the Reset line down and high, waits for the entered time.
This command typically can be used to execute the firmware programmed in the device.

#TPCMD READ_MEM8

Syntax: `#TPCMD READ_MEM8 <Address> <Byte Count>`

<Address>	Address in HEX format (i.e., 0x52002020)
<Byte Count>	Byte count in decimal format (i.e., 8 -> eight bytes)

Prerequisites: none

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C.F. 01697470936
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Description: Read memory byte per byte from target MSPM0 device

Note: This command prints into Terminal and Real Time Log

Examples: Correct command execution: 😊

```
---#TPCMD READ_MEM8 0x52002020 8
Read[0x52002020]: 0xF0
Read[0x52002021]: 0xAA
Read[0x52002022]: 0x16
Read[0x52002023]: 0x14
Read[0x52002024]: 0x00
Read[0x52002025]: 0x00
Read[0x52002026]: 0x00
Read[0x52002027]: 0x00
Time for Read Mem: 0.002 s
```

#TPCMD READ_MEM16

Syntax: `#TPCMD READ_MEM16 <Address> <16-bit Word Count>`

<Address>	Address in HEX format (i.e., 0x52002020)
<16-bit Word Count>	16-bit Word count in decimal format (i.e., 4 -> four 16-bit words)

Prerequisites: none

Description: Read memory 16-bit word per 16-bit word from target MSPM0 device

Note: This command prints into Terminal and Real Time Log

Examples: Correct command execution: 😊

```
---#TPCMD READ_MEM16 0x52002020 4
Read[0x52002020]: 0xAAF0
Read[0x52002022]: 0x1416
Read[0x52002024]: 0x0000
Read[0x52002026]: 0x0000
Time for Read Mem: 0.002 s
```

#TPCMD READ_MEM32

Syntax: `#TPCMD READ_MEM32 <Address> <32-bit Word Count>`

<Address>	Address in HEX format (i.e., 0x52002020)
<32-bit Word Count>	32-bit Word count in decimal format (i.e., 2 -> two 32-bit words)

Prerequisites: none

Description: Read memory 32-bit word per 32-bit word from target MSPM0 device

Note: This command prints into Terminal and Real Time Log

Examples: Correct command execution: 😊

```
---#TPCMD READ_MEM32 0x52002020 2
Read[0x52002020]: 0x1416AAF0
Read[0x52002024]: 0x00000000
Time for Read Mem: 0.002 s
```

#TPCMD DISCONNECT

`#TPCMD DISCONNECT`

Disconnect function. Power off and exit.

HQ and Registered Office
Via Giovanni Agnelli 1
33083 Villotta di Chions (PN) Italy
Società Unipersonale

Capitale sociale €102.040
P.I. 01697470936
C.F. 01697470936
REA PN-97255

D-U-N-S® 51-724-9350
T + 39 0434 421 111
F + 39 0434 639 021

→smh-tech.com

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TEXAS INSTRUMENTS MSPM0 Driver Examples

Here you can see a complete example of TEXAS INSTRUMENTS MSPM0 projects.

1 – TEXAS INSTRUMENTS MSPM0 64KB example Commands

MSPM0L1306

```
#TCSETPAR ENTRY_CLOCK 4000000
#TCSETPAR PLL_ENABLED YES
#TCSETPAR PROTCLK 37500000
#TCSETPAR PWDOWN 100
#TCSETPAR PWUP 100
#TCSETPAR RSTDOWN 100
#TCSETPAR RSTDRV OPENDRAIN
#TCSETPAR RSTUP 100
#TCSETPAR VPROG0 3300
#TCSETPAR CMODE SWD
#TPSETSRC 64KB.frb
#TPSTART
#TPCMD CONNECT
#TPCMD MASSERASE F
#TPCMD BLANKCHECK F
#TPCMD PROGRAM F
#TPCMD VERIFY F R
#TPCMD VERIFY F S
#TPCMD DISCONNECT
#TPEND
```

1 – TEXAS INSTRUMENTS MSPM0 64KB example Real Time Log

```
---#TPCMD CONNECT
Protocol selected SWD.
Entry Clock is 4.00 MHz.
Trying Reset Impulse connect procedure.
IDCODE: 0x6BA02477.
Designer: 0x23B, Part Number: 0xBA02, Version: 0x6.
ID-Code read correctly at 4.00 MHz.
JTAG-SWD Debug Port enabled.
Scanning AP map to find all APs.
AP[0] IDR: 0x84770001, Type: AMBA AHB3 bus, Description: MCPUSS debug AP.
AP[1] IDR: 0x002E0001, Type: AMBA AHB3 bus, Description: Configuration AP.
AP[2] IDR: 0x002E0000, Type: JTAG connection, Description: Security AP.
AP[3] IDR: 0x002E0003, Type: MEM-AP bus, Description: EnergyTrace™ AP.
AP[4] IDR: 0x002E0002, Type: AMBA APB2 or APB3 bus, Description: Power AP.
AP[0] ROM table base address 0xF0000000.
CPUID: 0x410CC601.
Implementer Code: 0x41 - [ARM].
Found Cortex M0+ revision r0p1.
Program counter value is 0x01000004.
Cortex M0+ Core halted [0.001 s].
Device configuration:
 * Flash main size: 64 KiB.
 * Flash main bank number: 1.
 * SRAM size: 4 KiB.
 * Data Flash size: 0 KiB.
 * Manufacturer ID: 0x017 - Texas Instruments.
 * Part Number ID: 0xBB82.
 * Version ID: 0x1.
PLL enabled using internal oscillator.
Requested Clock is 37.50 MHz.
Generated Clock is 37.50 MHz.
Good samples: 3 [Range 5-7].
IDCODE: 0x6BA02477.
Designer: 0x23B, Part Number: 0xBA02, Version: 0x6.
ID-Code read correctly at 37.50 MHz.
Time for Connect: 0.118 s.
>|
---#TPCMD MASSERASE F
Time for Masserase F: 0.007 s.
>|
```


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33083 Villotta di Chions (PN) Italy
Società Unipersonale

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C.F. 01697470936
REA PN-97255

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F + 39 0434 639 021

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```
---#TPCMD BLANKCHECK F
Time for Blankcheck F: 0.011 s.
>|
---#TPCMD PROGRAM F
Time for Program F: 0.423 s.
>|
---#TPCMD VERIFY F R
Time for Verify Readout F: 0.030 s.
>|
---#TPCMD VERIFY F S
Time for Verify Checksum 32bit F: 0.010 s.
>|
---#TPCMD DISCONNECT
>|
```

1 – TEXAS INSTRUMENTS MSPM0 64KB example Programming Times

Operation	Timings FlashRunner 2.0
Time for Connect	0.118 s
Masserase Flash	0.007 s
Blankcheck Flash	0.011 s
Program Flash	0.423 s
Verify Readout Flash	0.030 s
Verify Checksum Flash	0.010 s
Cycle Time	**00:00.654 s**

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33083 Villotta di Chions (PN) Italy
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REA PN-97255

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T + 39 0434 421 111
F + 39 0434 639 021

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TEXAS INSTRUMENTS MSPM0 Driver Changelog

Info about driver version 5.00 - 15/09/2023
First official version for driver MSPM0.
Supported TEXAS INSTRUMENTS MSPM0L series.

Info about driver version 5.01 - 15/02/2024
Supported MSPM0Gx series.
Add procedure to unlock the device into `#TPCMD CONNECT` command.
Added `#TCSETPAR CONNECT_UNLOCK` command to perform special SWD connect procedure through Mailbox.
Added PLL for all MSPM0 devices.

Info about driver version 5.02 - 13/06/2024
Internal driver updates for increase performances.

Info about driver version 5.03 - 04/07/2024
Added `#TPCMD UPDATE_NONMAIN` command for all MSPM0L and MSPM0G devices to update the NONMAIN memory more safely.

Info about driver version 5.04 - 05/09/2024
Supported MSPM0Cx series.

Info about driver version 5.05 - 24/10/2024
Managed correctly WWDT watchdog and upgraded connect procedure.

Info about driver version 5.06 - 22/01/2025
Updated driver for MSPM0x with 2KB SRAM.

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Via Giovanni Agnelli 1
33083 Villotta di Chions (PN) Italy
Società Unipersonale

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